AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 4. (Cancelled):

5 (Currently Amended) A method of processing a semiconductor device according to claim 21, wherein ~~said~~ information on the exposure distortion caused by the first exposure tool and information on the exposure distortion caused by the second exposure tool used in said step of rendering the exposure of the second overlay measurement mark and second pattern by using the second exposure tool fitted up with the second mask are stored in a memory in advance.

6 (Previously Presented) A method for processing a semiconductor device according to claim 21 further including the step of displaying information on the overlay accuracy between the first circuit pattern and the second circuit pattern.

7. – 20. (Canceled)

21 (Previously Presented) A method of processing a semiconductor device comprising the steps of:

applying photo-resist to a surface of a substrate to be processed;

rendering exposure of first layer overlay marks and a first layer circuit pattern to the substrate coated with the photo-resist by using a first exposure tool which is fitted up with a first mask;

processing the substrate, which has been rendered with the exposure of the first layer overlay marks and the first layer circuit pattern, to form thereon first layer overlay marks and a first layer circuit pattern;

applying photo-resist to the surface of the substrate on which the first layer overlay marks and the first layer circuit pattern have been formed;

rendering exposure of second layer overlay marks and a second layer circuit pattern to the substrate coated with the photo-resist by using a second exposure tool which is fitted up with a second mask;

processing the substrate, which has been rendered with the exposure of the second layer overlay marks and the second layer circuit pattern, to form thereon second layer overlay marks and a second layer circuit pattern; and

wherein said step of rendering the exposure of the second layer overlay mark and the second layer circuit pattern by using the second exposure tool fitted up with the second mask includes, beforehand, the steps of calculating matching error in circuit pattern areas between exposure distortions of first-layer and second-layer circuit pattern areas being smaller than an exposure field, calculating matching error at overlay mark positions between exposure distortions of first-layer and second-layer overlay mark positions, calculating a modification value which relates both said matching errors, calculating a first exposure condition correction value based on an overlay measurement result which is a result of actual exposure by said second exposure tool by positioning with reference to overlay marks, and modifying said

calculated first exposure condition correction value with said modification value to obtain a second exposure condition correction value for rendering the exposure by using said second exposure tool.

22. (New) A method of processing a semiconductor device according to claim 21, wherein said second exposure condition correction value to be modified in said step of rendering of the exposure of the second layer overlay mark and the second layer circuit pattern by using the second exposure tool fitted up with the second mask, includes any of positional shift, rotation and magnification factor of a second exposure field in reference to said second overlay marks.

23. (New) A method of processing a semiconductor device comprising the steps of:

applying photo-resist to a surface of a substrate to be processed;

rendering exposure of first layer overlay marks and a first layer circuit pattern to the substrate coated with the photo-resist by using a first exposure tool which is fitted up with a first mask;

processing the substrate, which has been rendered with the exposure of the first layer overlay marks and the first layer circuit pattern, to form thereon first layer overlay marks and a first layer circuit pattern;

applying photo-resist to the surface of the substrate on which the first layer overlay marks and the first layer circuit pattern have been formed;

rendering exposure of second layer overlay marks and a second layer circuit pattern to the substrate coated with the photo-resist by using a second exposure tool which is fitted up with a second mask; and

processing the substrate, which has been rendered with the exposure of the second layer overlay marks and the second layer circuit pattern, to form thereon second layer overlay marks and a second layer circuit pattern;

wherein said step of rendering the exposure of the second layer overlay mark and the second layer circuit pattern by using the second exposure tool fitted up with the second mask includes, beforehand, the steps of calculating matching error at overlay mark positions between exposure distortions of first-layer and second-layer overlay mark positions being indicated as having a disparity between said first and said second exposure tools or said first and said second masks, calculating a first exposure condition correction value based on an overlay measurement result which is a result of actual exposure by said second exposure tool by positioning with reference to overlay marks, and modifying said calculated first exposure condition correction value by using said calculated matching error at overlay mark positions to obtain a second exposure condition correction value for rendering the exposure by using said second exposure tool.

24. (New) A method of processing a semiconductor device according to claim 21, wherein said step of rendering the exposure of the second layer overlay marks and the second layer circuit pattern by using the second exposure tool fitted up with the second mask further includes the steps of calculating said exposure distortions of first-layer and second-layer circuit pattern areas and said exposure

distortions of first-layer and second-layer overlay mark positions based on a first field distortion of said exposure field of said first exposure tool, a second field distortion of said exposure field of said second exposure tool and product information including data of circuit pattern area coordinate and overlay mark positions.

25. (New) A method of processing a semiconductor device according to claim 21, wherein said step of rendering the exposure of the second layer overlay mark and the second layer circuit pattern by using the second exposure tool fitted up with the second mask further includes the steps of calculating said exposure distortions of first and second circuit pattern areas and said exposure distortions of first and second overlay mark positions based on a first field position error of said exposure field of said first mask, a second field position error of said exposure field of said second mask and product information including data of circuit pattern area coordinate and overlay mark positions.

26. (New) A method of processing a semiconductor device according to claim 21, wherein said step of rendering the exposure of the second layer overlay mark and the second layer circuit pattern by using the second tool fitted up with the second mask includes further the steps of calculating said exposure distortions of the first circuit pattern area and said exposure distortions of the first overlay mark positions based on a first field distortion of said exposure field of said first exposure tool, a first field position error of said exposure field of said first mask and product information including data of circuit pattern area coordinate and overlay measurement mark positions, and calculating said exposure distortions of a second

circuit pattern area and said exposure distortions of second overlay mark positions based on a second field distortion of said exposure field of said second exposure tool, a second field position error of said exposure field of said second mask and said product information.

27. (New) A method of processing a semiconductor device comprising the steps of:

applying photo-resist to a surface of a substrate to be processed;

rendering exposure of first layer overlay marks and a first layer circuit pattern to the substrate coated with the photo-resist by using an exposure tool which is fitted up with a first mask;

processing the substrate, which as been rendered with the exposure of the first layer overlay marks and the first layer circuit pattern, to form thereon first layer overlay marks and a first layer circuit pattern;

applying photo-resist to the surface of the substrate on which the first layer overlay marks and the first layer circuit pattern have been formed;

rendering exposure of a second layer overlay marks and a second layer circuit pattern to the substrate coated with the photo-resist by using the exposure tool which is fitted up with a second mask; and

processing the substrate, which has been rendered with the exposure of the second layer overlay marks and the second layer circuit pattern, to form thereon second layer overlay marks and a second layer circuit pattern;

wherein said step of rendering the exposure of the second layer overlay mark and the second layer circuit pattern by using the exposure tool fitted up with the

second mask includes, beforehand, the steps of calculating a matching error in a circuit pattern area between exposure distortions of first-layer and second-layer circuit pattern areas which are smaller than an exposure field, calculating matching error at overlay mark positions between exposure distortions of first-layer and second-layer overlay mark positions, calculating a modification value which relates both said matching errors, calculating a first exposure condition correction value based on an overlay measurement result which is a result of actual exposure by said second exposure tool by positions with reference to said overlay mark, and modifying said calculated first exposure condition correction value with said modification value to obtain a second exposure condition correction value for rendering the exposure by using said exposure tool.

28. (New) A method of processing a semiconductor device according to claim 27, wherein said step of rendering the exposure of the second overlay mark and the second pattern by using the exposure tool fitted up with the second mask includes further steps of calculating said exposure distortions of first and second circuit pattern areas and said exposure distortions of first and second overlay mark positions based on a first field position error of said exposure field of said first mask, a second field position error of said exposure field of said second mask and product information including data of circuit pattern area coordinate overlay mark positions.

29. (New) A method of processing a semiconductor device according to claim 21, wherein said matching error in the circuit pattern area calculated in the steps of calculating matching error and said matching error at overlay mark positions

calculated in the step of calculating matching error indicate disparity between said first and said second exposure tools or said first and said second masks.

30. (New) A method for processing a semiconductor device according to claim 23, wherein said exposure condition of the second circuit pattern to be modified in said step of rendering the exposure of the second overlay measurement mark and second circuit pattern by using the second exposure tool fitted up with the second mask includes any of the positional shift, rotation and magnification factor of the second circuit pattern resulting from the rendition of exposure on the surface of the substrate.

31. (New) A method for processing a semiconductor device according to claim 23, wherein said information on the exposure distortion caused by the first exposure tool and information on the exposure distortion caused by the second exposure tool used in said step of rendering the exposure of the second overlay measurement mark and second circuit pattern by using the second exposure tool fitted up with the second mask are stored in a memory in advance.

32. (New) A method for processing a semiconductor device according to claim 23, further including the step of displaying information on the overlay accuracy between the first circuit pattern and the second circuit pattern.

AMENDMENTS TO THE DRAWINGS

The attached sheets of drawing include changes for Figs. 5-7. These sheets, which include Figs. 5-7, replace the original sheets including Figs. 5-7. Regarding this, marks have been provided at appropriate locations in the drawings to correspond to marks discussed in the specification, as will be discussed in the Remarks of this Amendment.